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3D backside processing

Page 45

- Plasma dicing
- FOWLP advances
- Packaging trends & update
- Emerging automotive applications
- Improving yield and reliability in AOI
- Impact of wafer-based packaging on the supply chain

Plasma dicing methods for thin wafers

By Christopher Johnston [Plasma-Therm LLC]

The concept of employing deep silicon etch technology to dice wafers is called plasma dicing. The technology delivers very high dicing quality results and design flexibility. As a parallel process, it dices the entire wafer at the same time without die size sensitivity. From a cost perspective, plasma dicing is very attractive for thin and small devices. Larger products benefit from the higher dicing quality attained and limitless wafer layout designs. Several methods for plasma dicing are offered today to address risks with thin wafers and overcome integration challenges for various devices. As a consequence of product diversity, plasma dicing processes have various levels of complexity, costs and limitations. Upon exploring the various process options, key factors to consider are wafer preparation and support, dicing process and post-processes.

Today, semiconductor devices performance, packaging and cost requirements are demanding higher wafer dicing quality, flexibility and speed. Thinner and smaller packaging trends are limited by blade and laser dicing methods due to the mechanical and thermal stress and longer process times for smaller devices. Plasma dicing is a chemical process that offers significant advantages as described in Figure 1. This article will examine the different approaches to perform plasma dicing: plasma dicing before grind (DBG), plasma dicing after grind (DAG), laser grooving for plasma dicing, and plasma dicing on tape (PDOT).

As the need to increase the number of die per wafer continues to grow with each product generation, the spacing between die is limited by the precision and dicing quality of mechanical dicing systems. Such systems have numerous dynamic forces that are very difficult to control in addition to the variation from system to system and processing materials. As a result, the variation in die size and defect control area limit wafer layout designs. Squeezing accuracy performance from mechanical systems can be an expensive battle. However, the yield risk may be so high that extensive process control systems and metrologies must be employed. Plasma dicing offers an opportunity to regain process margins with near perfect dicing accuracy (Figure 2). It may be possible that delivering ultra-low variation products to downstream processes could have a positive "snowballing" effect with alignment, placement, bonding, dispensing errors, and defects as a secondary benefit.

Plasma dicing methods

There are four main approaches that have been developed to perform plasma dicing. The process flows for each method are explained in Table 1:

- DBG with and without additional mask
- DAG w/ additional mask
- Laser grooving followed by plasma dicing
- PDOT

DAG and DBG differences

In standard dicing process flows, dicing occurs after the wafer grinding or thinning step (i.e., DAG). DAG processes are used for >35µm thick wafers, as shown in Table 2. Ultra-thin wafer DAG may require trimming the wafer edge bevel to reduce risk of wafer edge damage. To achieve wafer thicknesses <50µm [1], the DBG process is more common. DBG

Lower Cost of Ownership for small die and thin wafers	•Thinner wafers = faster dicing time (i.e. 50um thick wafer < 3 minutes for dicing)
Maximized die per wafer or additional functionality per area	•Optimized die placement, non-orthogonal streets •Less wafer starts, more capacity
No shape, size or layout constraints	•Freedom to dice any shape, multi-product wafers •Rethink/relocate test/alignment areas
Higher die strength	•No chipping or micro-cracking •No mechanical or thermal stress
Highest accuracy	•Die size variation determined by the mask

Figure 1: Benefits of plasma dicing.

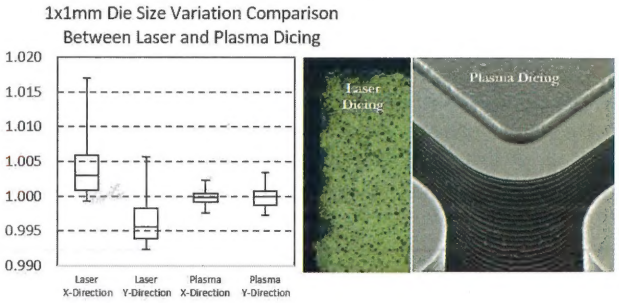

Figure 2: Die size variation between laser and plasma dicing. SOURCE: ON Semiconductor, Arizona, 2014

Thin Wafer Plasma Dicing Process	Thinning			Dicing							Thinning		
				Laser Grooving			Plasma Dicing						
	BG Tape Lamination	Wafer Thinning	Wafer Mounting	Wafer Coating	Laser Ablation	Wafer Cleaning	Litho Mask	Mask Exposure	Etching	Ashing	DBG Tape Lamination	Wafer Thinning	Wafer Mounting
Plasma DBG									•		•	•	•
Plasma DBG*							•	•	•	•	•	•	•
Plasma DAG*	•	•	•				•	•	•	•			
Grooving + Plasma DAG	•	•	•	•	•	•			•	•			
PDOT	•	•	•						•				

*Requires an additional mask

Table 1: Plasma dicing process flows.

Dicing Process Per Wafer Thickness		
Process	Wafer Thickness	Kerf Width
DAG	>35um	>4um*
DBG	<50um	>30um**

*Achieved with Plasma Dicing on Tape Process
**Achieved with special Backside Grind Tape

Table 2: Dicing process per wafer thickness.

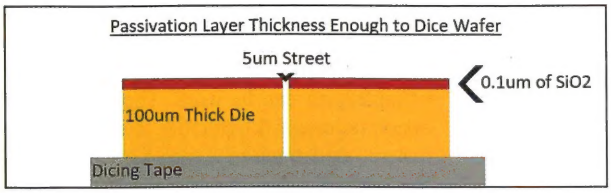

Figure 3: 1000 to 1, SiO_2 mask-to-silicon selectivity with the PDOT process.

Plasma Dicing Cost and Quality Comparison

Plasma Dicing Process	Setup Costs	Dicing Costs	Cleaning Costs	Dicing Quality	Kerf With
Plasma DBG w/o Additional Mask	None	Special Materials	In-situ	Competitive	>30um
Plasma DBG w/ Additional Mask	High	Special Materials	Separate System	Competitive	>30um
Plasma DAG w/ Additional Mask	High	Special Materials	In-situ	Competitive	>20um
Laser Grooving + Plasma DAG	Medium	Multiple steps	Separate System	Laser Damage	>30um
Plasma Dicing on Tape (PDOT)	None	Low	In-situ	Competitive	>4 um

Table 3: Plasma dicing process cost and quality comparison.

reduces some of the damage risks with mounting ultra-thin wafer on tape frames. In the DBG process, wafer dicing occurs during the wafer grind process exposing the partial kerf or blind etch done during the dicing step.

Successful plasma dicing requires proper support and wafer preparation. In the plasma DBG process, the full thickness wafers are partially diced and maintain enough rigidity for the next process steps without any additional support. Partially etched wafers require wide kerfs for the special backside grind tape adhesive to penetrate into the kerf to reduce damage during the wafer separation in the grind and mounting process. DAG process wafer support is required to hold the die together after dicing. The plasma etching process occurs in a vacuum environment and at temperatures that may cause problems for standard dicing tapes. Some of the problems that arise are wafer and chamber contamination, tape damage, or residue. Systems not compatible with standard dicing tapes may require special vacuum and high-temperature compatible tapes or other forms of tape protection.

Wafer preparation for plasma dicing

The areas that are not to be etched by the dicing process may need to be protected or covered by a mask [2]. Depending on the aggressiveness of the etching system, bumps, pads, any metals or materials prone to damage or contamination may need protection. For most dry etch applications, the areas left unmasked, such as the spacing between die, will be attacked by the plasma. The mask thickness is determined by the selectivity, etch rate of the mask material versus the silicon, and the silicon amount to be diced. The costs to prepare wafers for plasma dicing can be overwhelming for some processes. It is important to note that some or all of the setup costs for plasma dicing can be eliminated with a high-selectivity dicing system used in the PDOT process. The plasma Singulator™ system by Plasma-Therm is a high-selectivity plasma dicing system requiring no additional mask protection. The PDOT process employs the passivation layer [3] as the mask (example shown in Figure 3) to dice the wafer.

The dry etch process requires direct access to open the silicon in the streets for the plasma to dice the wafer. This access may include opening the mask through exposure or a laser ablation process. Non-silicon structures in the streets, test element groups (TEGs), alignment features, or process control monitoring (PCM) structures [4] interfere with the plasma reaching the bulk silicon underneath. Street structures are commonly removed via blade dicing or laser grooving processes that increase yield risks caused by the mechanical and thermal damage that was induced. The street structures take up valuable wafer real estate, which could be used for more devices. The capability of plasma to dice any shape and extreme narrow features is enabling more and more efficient wafer designs.

Plasma dicing process

Process gases, SF_6 and C_4F_8 are used in the time-multiplex alternating etching/deposition cycles to etch the exposed silicon and to control the vertical anisotropic profile. For the DBG process, partial etching is completed when a predetermined number of cycles reaches the desired depth. In the DAG process, the completion of the dicing process is determined once all exposed silicon is etched. The etched silicon byproduct emission is monitored by an optical emission endpoint control system. Once the byproduct signal disappears, the street silicon has been etched and the dicing process stops. Endpoint detection becomes very challenging for wafers with small amounts of exposed silicon area and may require more sophisticated detection systems.

Post-dicing cleaning

Once the etching process ends, there may be residue materials that require stripping or cleaning. The deposited polymers that control the etch profile, may cause corrosion or affect downstream processes and require stripping. Some plasma dicing systems include an in situ polymer stripping in the same process chamber. Other processes require external cleaning systems to remove left-over mask materials, as well as etching polymers (see Table 3).

Summary

Advanced packaging trends are becoming so diverse that not one dicing solution can solve all challenges. Wafer layouts and die designs are formed around manufacturing capabilities. These design rules will continue to evolve as new manufacturing capabilities are qualified. The wafer preparation steps have the biggest cost impact and the point of definition in the process flow are device-specific. Materials such as oxides, photoresist polyimides, photosensitive polyimides, metals, metal oxides and water- soluble protective materials have been used with success. To open the silicon for plasma dicing, a number of strategies can be used. The lowest cost option technique is to remove the non-etchable material as part of the process flow or redesign the test structures to eliminate the problem. The ability of plasma dicing to etch very fine features, high-aspect ratios and any shape will enable creative solutions around test structures. This design approach is already implemented in small die products such as RFIDs, LEDs and power devices employing plasma dicing techniques to solve quality/reliability issues, reduce dicing cost-of-ownership (CoO), and improve die per wafer outputs. Plasma dicing is a competitive advantage that is soon to spread to more applications as the first 300mm wafer production systems are delivered in 2016.

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Biography

Christopher Johnston received his Electronics Engineer Degree from Devry U., MBA, MPM from Keller and is a Business Development Manager at Plasma-Therm LLC; email christopher.johnston@plasma-therm.com